REMARKS

Claims 1 through 15 are pending in this Application. Applicant acknowledges, with appreciation, the Examiner's allowance of claims 1 through 3, and the Examiner's indication that claims 6, 7, 9, 10, 12 and 13 contain allowable subject matter. Accordingly, the only remaining issues pivot about the patentability of claims 4, 5, 8, 11, 14 and 15.

Claims 4, 5, 7, 12 and 13 have been amended. Care has been exercised to avoid the introduction of new matter. Indeed, adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, the depicted embodiments and related discussion thereof in the written description of the specification. Applicant submits that the present Amendment does not generate any new matter issue.

Claims 4, 5 and 8 were rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Nikai et al.

In the statement of the rejection the Examiner referred to Figs. 1 through 3 of Nikai et al. asserting the disclosure of a signal conversion unit corresponding to that claimed. This rejection is traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc., 329 F.3d 1358 (Fed. Cir. 2003); Crown Operations International Ltd. v. Solutia Inc., 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002).* There are significant differences between the claimed circuit and that

disclosed by Nikai et al. that scotch the factual determination that Nikai et al. disclose a circuit identically corresponding to that claimed.

Specifically, the circuits defined in each of independent claims 5 and 6 comprise, *inter alia*, a second adjustment unit. This second adjustment unit **cancels** a temporary variation which is caused in the values of the input signal as a result of setting the reference signal during conversion of the input signal to a target signal (claim 4) or which is caused in values of the input analog voltage during A-D conversion as a result of setting a reference signal (claim 5). No such systems comprising a second adjustment unit that **cancels** a temporary variation are disclosed or suggested by Nikai et al.

Specifically, Nikai et al. disclose a system wherein that a first intermediate reference voltage VRT1 is obtained by connecting a resistor having a resistance value which is n times (that of) the resistor R between a node N31 and node N35 (referring to column 24, lines 39 through 65). As a result of this arrangement, the ratio of the reference voltage range RA1 of the sub-A/D converter 9 to the reference voltage range RD1 of the D/A converter 10 is set to 1:2 (column 26, lines 18 through 34). This ratio is **not** subject to variation. The reference voltage range of the sub-A/D and the reference voltage range of the D/A converter 10 can be independently set, respectively, thereby enabling arbitrarily setting the gains of the operational amplification circuits 11 and 13. In this way, the degree of freedom of the design is increased.

But Nikai et al. merely disclose that a **fixed** voltage-division arrangement at the input of the sub-A/D converter 9 adjusts the reference voltage range of the sub-A/D converter 9 so as to be adopted to the gain of the operational amplifier. Nikai et al. fail to disclose that the level of the reference signal is set **according to**, i.e., by examining or

referring to, the range of the input voltage. This is a significant difference between the claimed system and that disclosed by Nikai et al.

Moreover, it would appear that the Examiner equated the operation for **canceling** a variation in input voltage caused by the operation of the first adjustment unit according to the present invention with the operation of the subtracter 12 of the reference. However, the "offset" according to the present invention refers to the act of **cancellation** of a variation in the input voltage caused by adjusting the output of the A/D conversion unit. Thus, one having ordinary skill in the art reading the claimed invention would understand that the term "offset" means cancellation -- **not**, repeat **not**, "subtraction", which is the way the Examiner apparently interpreted the term "offset". Applicant would stress that claims must be interpreted through the eyes of one having ordinary skill in the art in light of, consistent with, and in the context of, the disclosed invention. *Dayco Products, Inc. v. Total Containment, Inc., 258 F.3d 1317, 59 USPQ2d 1489 (F.C. 2001); Atmel Corp. v. Information Storage Devices, Inc., 198 F.3d 1374, 53 USPQ2d 1225 (Fed Cir. 1999); In re Cortright, 165 F.3d1353, 49 USPQ2d 1464 (Fed. Cir. 1999); Toro Co. v. White Consolidated Industries, Inc., 199 F.2d 1295, 53 USPQ2d 1065 (Fed. Cir. 1999).* In this respect Applicant would refer to page 5 of the written description of the specification, line 2, as an example. At any rate, in order to expedite prosecution, the word "offsets" in claims 4 and 5 has been changed to "cancels". No such second adjustments unit which **cancels** a temporary variations in the input is disclosed or suggested by Nikai et al.

The above argued functionally significant differences between the claimed systems and the system disclosed by Nikai et al. undermine the factual determination that Nikai et al. disclose a system identically corresponding to those claimed. *Minnesota Mining &*

Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicant, therefore, submits that the imposed rejection of claims 4, 5 and 8 under 35 U.S.C. § 102 for lack of novelty as evidenced by Nikai et al. is not factually viable and, hence, solicits withdrawal thereof.

Claims 11, 14 and 15 were rejected under 35 U.S.C. §102 for lack of novelty as evidenced by McCarroll.

In the statement of rejection the Examiner referred to Fig. 1 of McCarroll, asserting the depiction of a circuit identically corresponding to that claimed. This rejection is traversed.

As previously pointed out, the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc., supra; Crown Operations International Ltd. v. Solutia Inc., supra.* Further, in imposing a rejection under 35 U.S.C. § 102, the Examiner must specifically identify wherein an applied reference is perceived to identically disclose each and every feature of a claimed invention. *In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).* That burden has not been discharged. Indeed, there is a significant difference between the signal conversion circuit defined in claim 11 and that disclosed by

McCarroll that scotches the factual determination that McCarroll discloses a signal conversion circuit identically corresponding to that claimed.

Specifically, the signal conversion unit defined in independent claim 11 comprises an A/D conversion unit and a "sample-and-hold unit which acquires and holds a value adjusted so that the input analog voltage to be acquired by said A-D conversion unit falls within a satisfactory range in terms of conversion performance thereof." No such sample-and-hold unit is disclosed or suggested by McCarroll.

It would appear that the Examiner attempted to equate the sample-and-hold circuits 15, 25, 35, 45 of McCarroll with the sample-and-hold circuit of the claimed invention. This interpretation of the claimed sample-and-hold circuit is not accurate. Specifically, the sample-and-hold circuits disclosed by McCarroll et al. only provide a comparing signal to the subtracter 16. They do **not**, repeat **not**, have the function as specified in claim 11, i.e., "... acquires and holds a value adjusted so that the input analog voltage to be acquired by said A-D conversion unit falls within a satisfactory range in terms of conversion performance thereof."

Applicant separately argues the patentability of **claim 14**. In addressing claim 14, the Examiner expressed the view that McCarroll discloses a circuit wherein the input analog value is inputted, as it is, to an analog-digital converter 11, and an adjusted value of the input analog value is inputted to a sample-and-hold circuit 15. A review of Fig. 1 of McCarroll, however, reveals that the Examiner's determination is not accurate. In short, McCarroll et al. neither disclose nor suggest a system wherein the input analog value is inputted, as it is, to the A-D conversion unit and an adjusted value of the input analog value is inputted to the sample-and-hold unit, as set forth in claim 14.

The above argued differences between the claimed circuit and the circuit disclosed by McCarroll undermine the factual determination that McCarroll discloses a circuit identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., supra; Kloster Speedsteel AB v. Crucible Inc., supra.* Applicant, therefore, submits that imposed rejection of claims 11, 14 and 15 under 35 U.S.C. § 102 for lack of novelty as evidenced by McCarroll is not factually viable and, hence, solicits withdrawal thereof.

Applicant, again, acknowledges appreciation for the Examiner's allowance of claims 1 through 3 and the Examiner's indication that claims 6, 7, 9, 10, 12 and 13 contain allowable subject matter. Based upon the arguments submitted *supra*, it should be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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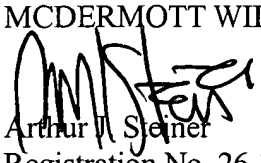

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WDC99 932694-1.065933.0048